

**PROCEDURE
FOR THE TESTING AND COMMISSIONING OF GRID-
CONNECTED PHOTOVOLTAIC SYSTEMS IN MALAYSIA**

**INVERTER SITE TESTS - PV PLANTS CONNECTED AT MEDIUM
VOLTAGE**



**SUSTAINABLE ENERGY DEVELOPMENT AUTHORITY (SEDA)
MALAYSIA**

2014

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1. INVERTER SITE TESTS

The inverter site tests are only meant for PV plants connected at medium voltage, which would normally be greater than 425 kWp in capacity.

The inverter site tests shall be conducted by the Competent Party recognised by SEDA Malaysia as stated at the end of the checklist whilst adhering to the provisions of all relevant laws and regulations.

The completed report for inverter site tests result must be submitted directly to SEDA Malaysia by the Competent Party.

The objective of carrying out the Inverter Site Tests is to assess the impact of the inverter output on the Grid. This will ascertain their suitability for use in Malaysia as well as confirm that the inverters meet the output parameters as claimed by the manufacturers. The tests must be carried out during the period prescribed for each test. During this period, inverter output must vary at least between 10% to 50% of rated output.

The Inverter Site Tests are as follows:

1. Power Factor Test
2. Harmonics Test
3. Voltage Fluctuation Test
4. Flicker Test
5. DC Current Injection Test
6. Anti-islanding Test
7. Steady State Voltage Measurement at Medium Voltage

1.1 POWER FACTOR TEST

Table 1.1 Power factor test						
Inverter ID						Date of inspection:
Inverter Description						(dd_mmm_yyyy)
Test point	<ul style="list-style-type: none"> Each inverter output terminal (for central inverters) Common output point from group of inverters (for string inverters) 					
Test condition	<ul style="list-style-type: none"> Switch off all other inverters (both at input & output) except the one which is under test. The recording for the test shall be done for at least six (6) day light hours. 					
Acceptable limit	<ul style="list-style-type: none"> Power Factor is > 0.85 lagging when inverter output is approximately 10 % of rated power. Power Factor > 0.9 lagging when inverter output is approximately 50 % of rated power. Both the above conditions must be tested and met 					
Use appropriate tools to measure and record						
Tables and Graphs	Plotted Graph for the entire monitoring period must be attached					
No	Inverter output approximately 10 %			Inverter output approximately 50 %		
	Output	Min pf	Measured pf	Output	Min pf	Measured pf
Inverter 1/Inverter Group 1		0.85			0.9	
Inverter 2/Inverter Group 2		0.85			0.9	
Inverter 3/Inverter Group 3		0.85			0.9	
Overall result (Please tick ✓ in the appropriate box)			Pass: <input type="checkbox"/>		Fail: <input type="checkbox"/>	
Comments:						

Signature	
Name	
Date	
Designation	(Competent party recognised by SEDA)

1.2 HARMONICS TEST

Table 1.2 Harmonics test																		
Inverter ID		Date of inspection: (dd_mmm_yyyy)																
Inverter Description																		
Test point	<ul style="list-style-type: none"> • Each inverter output terminal (for central inverters). • Common output point from group of inverters (for string inverters). 																	
Test condition	<ul style="list-style-type: none"> • Switch off all other inverters (both at input & output) except the one which is under test. • The recording for the test shall be done for at least six (6) day light hours. 																	
Acceptable limit	<ul style="list-style-type: none"> • Maximum THD Current is less than or equal to 5% at not more than 50% rated inverter output. • Individual Harmonics limited to the following at not more than 50% rated inverter output: <ul style="list-style-type: none"> • Current distortion limits (IEC 61727-2003 Table 1) <table border="1" data-bbox="646 1014 1396 1308"> <thead> <tr> <th>Odd harmonics</th> <th>Distortion limit (%)</th> </tr> </thead> <tbody> <tr> <td>3 – 9</td> <td>< 4.0</td> </tr> <tr> <td>11 – 15</td> <td>< 2.0</td> </tr> <tr> <td>17 – 21</td> <td>< 1.5</td> </tr> <tr> <td>23 – 33</td> <td>< 0.6</td> </tr> <tr> <th>Even harmonics</th> <th>Distortion limit (%)</th> </tr> <tr> <td>2 – 8</td> <td>< 1.0</td> </tr> <tr> <td>10 – 32</td> <td>< 0.5</td> </tr> </tbody> </table> 		Odd harmonics	Distortion limit (%)	3 – 9	< 4.0	11 – 15	< 2.0	17 – 21	< 1.5	23 – 33	< 0.6	Even harmonics	Distortion limit (%)	2 – 8	< 1.0	10 – 32	< 0.5
Odd harmonics	Distortion limit (%)																	
3 – 9	< 4.0																	
11 – 15	< 2.0																	
17 – 21	< 1.5																	
23 – 33	< 0.6																	
Even harmonics	Distortion limit (%)																	
2 – 8	< 1.0																	
10 – 32	< 0.5																	
Test duration																		
Tables and Graphs	<ul style="list-style-type: none"> • Tables to show the odd and even harmonics for each phase must be attached. • Plotted THD Graphs for each phase must be attached 																	
Overall result (Please tick ✓ in the appropriate box)	Pass: <input type="checkbox"/>	Fail: <input type="checkbox"/>																
Comments:																		

Signature	
Name	
Date	
Designation	(Competent party recognised by SEDA)

1.3 VOLTAGE FLUCTUATION TEST

Table 1.3 Voltage Fluctuation Test		
Inverter ID		Date of inspection: (dd_mmm_yyyy)
Inverter Description		
Test point	<ul style="list-style-type: none"> • Each inverter output terminal (for central inverters) • Common output point from group of inverters (for string inverters) 	
Test condition	<ul style="list-style-type: none"> • Central Inverter - Switch off all other inverters (both at input & output) except the one which is under test • String Inverter - Switch off all other Main Switch Board except the one which is under test • The test shall be conducted for at least two hours at the mid-day (12.00 noon – 2.00 pm) at one second intervals. • Plot of rms voltage against time shall be produced for each phase of each central inverter or group of string inverters 	
Acceptable Limit	<ul style="list-style-type: none"> • Max voltage fluctuation allowed is 6% from maximum to minimum of the biggest fluctuation during the test period 	
Test duration		
Overall result (Please tick ✓ in the appropriate box)	Pass: <input type="checkbox"/>	Fail: <input type="checkbox"/>
Comments:		

Signature	
Name	
Date	
Designation	(Competent party recognised by SEDA)

1.4 FLICKER TEST

Table 1.4 Flicker Test					
Inverter ID				Date of inspection: (dd_mmm_yyyy)	
Inverter Description					
Test point	LV Point of common coupling (PCC) or LV side of step-up transformer				
Test condition	<ul style="list-style-type: none"> • Monitor the Short Time Flicker (Pst) for 10 min • Monitor the Long Time Flicker (Plt) for 2 hours • The PQ Analyser should be set to flicker mode to record the data 				
Acceptable Limit	Should not exceed the limits defined by the maximum borderline irritation limits as below: <ul style="list-style-type: none"> • Pst < 1.0 • Plt < 0.8 				
Test point location	Time period	Phase details	Flicker		Remarks
			Limit	Measured	
	Pst	L1	< 1.0		
		L2	< 1.0		
		L3	< 1.0		
	Plt	L1	< 0.8		
		L2	< 0.8		
		L3	< 0.8		
Test duration					
Overall result (Please tick ✓ in the appropriate box)	Pass: <input type="checkbox"/>		Fail: <input type="checkbox"/>		
Comments:					

Remark: If Flicker Test failed, to check Grid connection that may lead to flickering problems

Signature	
Name	
Date	
Designation	(Competent party recognised by SEDA)

1.5 DC CURRENT INJECTION TEST

Table 1.5 DC Current Injection Test						
Inverter ID					Date of inspection: (dd_mmm_yyyy)	
Inverter Description						
Test point		<ul style="list-style-type: none"> Each inverter output terminal (for central inverters) Common output point from group of inverters (for string inverters) 				
Test condition		<ul style="list-style-type: none"> Switch off all other inverters (both at input & output) except the one which is under test. The maximum output of inverter shall be at 50% of rated output. 				
Acceptable limit		<ul style="list-style-type: none"> DC current is less than 1% of the rated output current from inverter for each phase 				
Set the current clamp to dc mode and record the data						
No.	Description	Measured current injection				Remarks
		L1	L2	L3	Pass/Fail	
1	Inverter 1 / Inverter Group 1					
2	Inverter 2 / Inverter Group 2					
3	Inverter 3 / Inverter Group 3					
Test duration						
Overall result (Please tick ✓ in the appropriate box)		Pass: <input type="checkbox"/>			Fail: <input type="checkbox"/>	
Comments:						

Signature	
Name	
Date	
Designation	(Competent party recognised by SEDA)

1.6 ANTI-ISLANDING TEST

Table 1.6 Anti-islanding test				
Inverter ID				Date of inspection: (dd_mmm_yyyy)
Inverter Description				
Test point		<ul style="list-style-type: none"> • Each inverter output terminal (for central inverters) • Common output point from group of inverters (for string inverters) 		
Test condition		<ul style="list-style-type: none"> • Switch off all other inverters (both at input & output) except the one which is under test. • Switch off the inverter under test and record the disconnection time. • Switch on the inverter under test and record the reconnection time. 		
Acceptable Limit		<ul style="list-style-type: none"> • Loss of grid supply <ul style="list-style-type: none"> • Maximum disconnection time is 0.6 s • Reconnection with grid supply restored <ul style="list-style-type: none"> • Minimum 300 s (5 minutes) for MV • Minimum 120 s (2 minutes) for LV • If the inverter cannot meet the reconnection time requirement, a timer relay must be included 		
No.	Description	Disconnection time	Reconnection time	Remarks
1	Inverter 1			
2	Inverter 2			
Overall result (Please tick ✓ in the appropriate box)		Pass: <input type="checkbox"/>		Fail: <input type="checkbox"/>
Comments:				

Signature	
Name	
Date	
Designation	(Competent party recognised by SEDA)

1.7 STEADY STATE VOLTAGE MEASUREMENT OF MEDIUM VOLTAGE

Table 1.7 Steady state voltage measurement of Medium Voltage

Inverter ID		Date of inspection: (dd_mmm_yyyy)
Inverter Description		
Test point		
Test condition	<ul style="list-style-type: none"> The test shall be conducted for a minimum of six day light hours at one minute intervals. Max voltage fluctuation allowed is $\pm 5\%$ of nominal 	
Test duration		
Overall result (Please tick ✓ in the appropriate box)	Pass: <input type="checkbox"/>	Fail: <input type="checkbox"/>
Comments:		

Signature	
Name	
Date	
Designation	(Competent party recognised by SEDA)

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